

Author [Venkateswarlu, P.](#); [Hudait, M. K.](#); [Krupanidhi, S. B.](#)

Author Affiliation Solar Panels Div., ISRO Satellite Centre, Bangalore, India

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Current transport study of Au/n-GaAs Schottky diodes on Ge substrate at low temperatures

P. Venkateswarlu^{1,2}, M. K. Hudait², and S. B. Krupanidhi²

¹Solar Panels Division, ISRO Satellite Centre, Bangalore 560 017, INDIA

²Materials Research Centre, Indian Institute of Science, Bangalore 560 012, INDIA

ABSTRACT: Au Schottky diodes were made on epi-GaAs grown over Ge substrate by metal-organic vapor phase epitaxy (MOVPE) technique. The current-voltage (I-V) characteristics were carried out at temperatures ranging from 80 K to 300 K and the parameters such as: reverse saturation current, ideality factor, zero-bias barrier height and Richardson constant were determined to assess the quality of the epi-GaAs material. With the decrease of temperature, the ideality factor increases while the zero-bias barrier height decreases and the observed results are explained based on the existing transport theories.

1.0 INTRODUCTION:

GaAs/Ge heterostructures are extensively used in many applications such as single and multi junction solar cells, Heterojunction Bipolar Transistors and Schottky barrier cells. When GaAs is grown as a film on Ge by MOVPE or MBE, it poses few problems like the formation of antiphase domains (APDs) in the epilayer, the introduction of misfit dislocations and cross diffusion of elements from Ge to GaAs and vice-versa. The large density of dislocations present in GaAs/Ge substrate is a major problem and it is necessary to understand the electrical activity of the defects. Hence, an attempt has been made in this paper to present some studies dealing with the I-V characteristics and current transport mechanisms of Au on GaAs/Ge Schottky diodes in the temperature range of 80 to 300 K.

2.0 EXPERIMENTAL PART:

Si-doped n-type GaAs film of 3 micron thick was grown on (100) oriented 2° off-cut towards [110] direction of Sb doped ($2 \times 10^{17}/\text{cc}$) n+ Ge substrate using low pressure metal-organic vapor phase epitaxy (LP-MOVPE) technique. Au Schottky contacts were made on front side using physical mask and thermal evaporation technique. The current-voltage (I-V) characteristics of the diodes were measured from room temperature to 80 K in steps of 10 K using an automated arrangement consisting of Keithley made source measuring unit SMU 236, a PC486 and a probe station and LN₂ cryostat. Capacitance-voltage (C-V) measurements were done at room temperature using capacitance meter at 1 MHz frequency and the barrier height measured was 0.776 eV and the carrier concentration of the grown n-type epitaxial layer was determined as $1.274 \times 10^{17}/\text{cc}$. This carrier concentration is further confirmed by means of Bio-rad electro-chemical C-V polaron profiler.

3.0 RESULTS AND DISCUSSION:

3.1 I-V Characteristics:

Fig. 1 shows the forward semi-log current-voltage (I-V) characteristics of Au-n GaAs/Ge Schottky diodes at different temperatures, ranging from 80 K to 300 K. According to Thermionic emission-Diffusion theory, the current transport across a Schottky diode is given by :

$$I = I_s \exp(qV/nkT) \quad \text{for } V > 3kT/q \quad \text{--- (1)}, \quad \text{where } I_s = A A^{**} T^2 \exp[-q\Phi_{b0}/kT] \quad \text{--- (2)}$$

V is the applied voltage drop across the semiconductor surface depletion layer and I_s the saturation current density. A is the diode area, A^{**} is the Richardson constant, Φ_{b0} is the zero-bias barrier height, n is the ideality factor, k is the Boltzmann constant, T is the temperature, and q is the charge.

Using eqns. (1) & (2) the values of n and Φ_{b0} of the diode at different temperatures were calculated considering $8.16 \text{ AK}^{-2}\text{cm}^{-2}$ as the value of A^{**} and plotted with temperature in Fig. 2. From Fig. 2, it is observed that the ideality factor increases with the decrease of temperature and the

increase is very slow up to 120 K and then increases steeply up to 80 K. The zero-bias barrier height decreases slowly with temperature up to 120 K and the further decrease is very steep up to 80 K. For an ideal Schottky diode, the zero-bias barrier height should increase with the decrease in temperature in accordance with the band gap variation with temperature. The zero-bias barrier height is showing an inverse behavior to the ideality factor variation.

To assess the quality of the grown GaAs film on Ge, the following existing models of conduction mechanisms have been applied to the observed low temperature I-V data of Au-n GaAs/Ge Schottky diodes. As per the Werner-Güttler model, the barrier height has a Gaussian distribution with a mean barrier height. The decrease in barrier height with reduction in temperature has been explained by the lateral distribution of the barrier height [1]. The Gaussian distribution of the barrier height yields Eq.(3) for the barrier height and the variation of ideality factor with the temperature is given by Eq. (4) as per potential fluctuation model of Werner-Güttler [1]

$$\Phi_{b0} = \Phi_{b\text{ mean}} - (\sigma_s^2 / 2kT) \quad \text{---(3)} \quad 1/n = 1 - \gamma + (q\zeta\sigma_s / kT) \quad \text{---(4)}$$

where, $\Phi_{b\text{ mean}}$ is the mean barrier height, σ_s is the standard deviation of the barrier distribution, γ and ζ are the voltage coefficients of barrier height. Using the experimentally determined values of n at different temperatures and the value of σ_s obtained from Eq. (3), the values of γ and ζ were obtained. The zero-bias barrier height and ideality factors were simulated using Eqs. (3) & (4) respectively and re-plotted along with the experimentally observed values in Fig. 2. From Fig. 2 it can be observed that the experimental and simulated zero-bias barrier heights are not matching and there is a large deviation in the temperature range from 120 K to 260 K. There is a deviation between the experimental and simulated ideality factors. We can conclude that the Werner-Güttler model is not adequate to explain the variation of the zero-bias barrier height and ideality factor with the temperature in the present case. Hence, we can conclude that the present investigated Schottky diodes do not have any inhomogenities in the grown n-type GaAs epitaxial film and indicates the excellent quality of the film.

According to Sullivan and Tung's model of lateral inhomogenities, Schmitsdroff et al [2] found a correlation between the zero-bias barrier height and the ideality factors. The extrapolation of the linear fit of zero-bias barrier height versus ideality factors gives a homogeneous barrier height of 0.78 eV at an ideality factor of about 1.01. This homogeneous barrier height is in close match with the

Fig. 1: The I-V characteristics of Schottky Diodes at different T

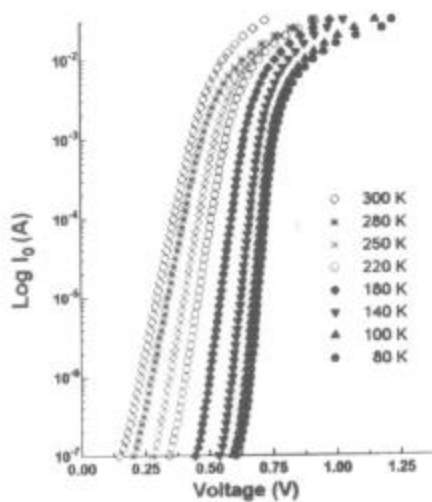
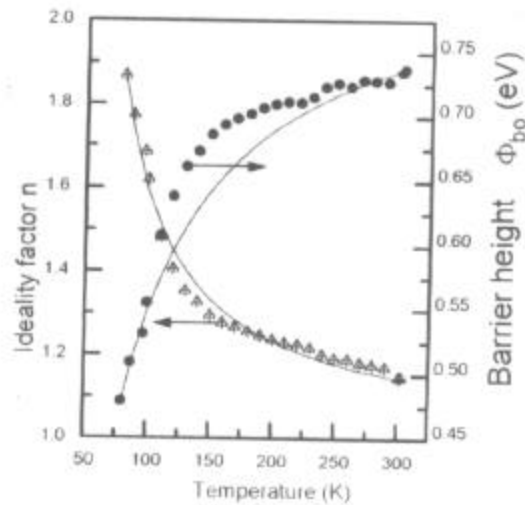


Fig. 2: The variation of Φ_{b0} and n with T. Solid lines- Simulated Φ_{b0} and n



effective barrier height ($\Phi_{bo}^{CT} = 0.776$ eV) obtained from (C-V) measurements. According to Schmitsdroff et al [2] larger the discrepancy between the homogeneous barrier height and the effective barrier height, the quality of the grown epilayer is poor. Based on the above proposed models, we can conclude that the present investigated Schottky diodes and the grown GaAs film do not have any lateral inhomogeneities and hence, the quality of the grown GaAs epilayer is excellent.

3.2 Effect of thermionic field emission :

If the current transport phenomenon is controlled by the thermionic field emission (TFE), the relation $I(V)$ is expressed as $I = I_s \exp(V/E_0)$ ---(5a) $E_0 = E_{00} \coth(qE_{00}/kT)$ ---(5b) where, E_{00} and E_0 are the semiconductor energies which are related to the transmission probability of the carrier through the barrier given as $E_{00} = \hbar/4\pi (N_D/m_e^* v_s)^{1/2} = 18.5 \times 10^{-15} (N_D/m_e^* v_s)^{1/2}$ ---(6). In the case of our Au/n-GaAs Schottky diode, the value of E_{00} turns out to be 7.13 meV. According to the transport theory, TFE dominates only when $E_{00} \approx kT$ and the value of E_{00} calculated using Eq.(6) is less than the kT at 80 K. But the barrier height lowering, $\Delta\Phi_{TFE}$ due to TFE is

$$\Delta\Phi_{TFE} = (1.5)^{2/3} (E_{00})^{2/3} (V_d)^{1/3} \quad \text{---(7) where } V_d \text{ is the built in potential.}$$

For a built in potential of 0.78 V and E_{00} value of 7.13 meV, the calculated barrier height lowering is 44.6 meV. This also can not account for the lowering of the barrier height.

Using the experimental values, E_0 versus kT/q was plotted and the plot gives the value of E_0 as 5.625 meV, which is less than the theoretically calculated value of 7.13 meV. If the curvature is considered at 120 K, it gives a very high characteristic energy, which explains the conduction mechanism as TFE. The values of $1/n$ were theoretically calculated using the following Eqn.(8)

$$1/n = (kT/q) [E_0 / (1-\beta)] \quad \text{---(8), where } \beta \text{ indicates the bias dependence of the barrier height.}$$

The experimentally observed values of $1/n$ were imposed on theoretically generated $1/n$ versus $1000/T$ plots in Fig. 3, to confirm the higher value of the characteristic energy. This plot provides a good check to know whether the conduction mechanism is TFE or TE. From Fig. 3, it is observed that E_{00} of 12 meV and β of 0.02 were obtained for a temperature range 80 K to 160 K. For a temperature range of 160 K to 300 K the value of E_{00} is around 17 meV. The higher value of E_{00} confirms that at lower temperatures, the diode conduction mechanism is TFE and TE-diffusion at higher temperature, although it has high base doping. The high characteristic energy has been related to several effects such as, the density of states and the electric field present on the surface of the semiconductor. The electric field near the semiconductor surface can be increased by any mechanisms such as, surface roughness at periphery, local pile of dopants, geometrical inhomogeneities due to crystal defects, presence of relatively thick interfacial insulator layer.

Fig. 3. $1/n$ vs. $1000/T$ curves (solid lines). (\circ) experimental Points. Dotted line gives $E_{00} = 12$ meV and $\beta = 0.02$

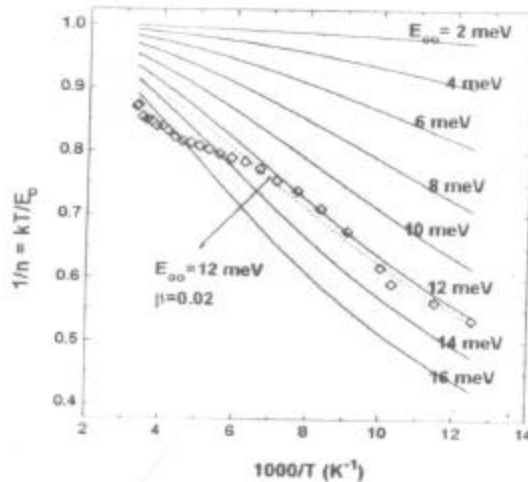
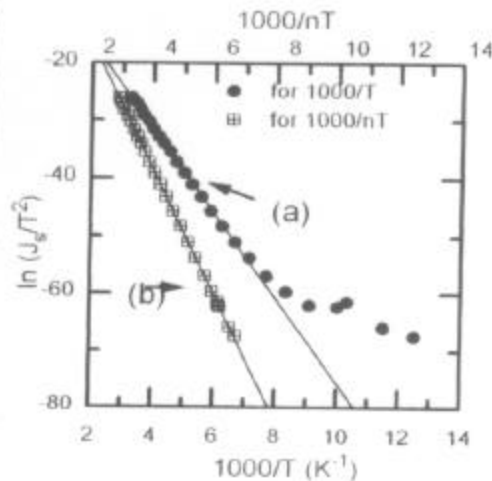


Fig. 4. The Richardson Plot (a) $\ln(J_s/T^2)$ vs. $1000/T$ and (b) $\ln(J_s/T^2)$ vs. $1000/nT$



3.3 Effect of generation-recombination:

Generation-recombination centers give rise to the value of ideality factor around 2 at room temperature. The measured values of n in the present case at 300 K and 80 K are 1.14 & 1.18 respectively. It is known from the literature [3] that the 2° off-oriented Ge substrates often gives the APDs and misfit dislocations during the growth of GaAs on Ge substrates. The epitaxial films are characterized by a number of techniques namely atomic force microscopy, low temperature photoluminescence spectroscopy, secondary ion mass spectroscopy, cross-section transmission electron microscopy, electrochemical capacitance voltage profiler [4], before fabricating the Au Schottky diodes. It was observed that [4] the quality of the film was excellent. Chand et al [5] studied the I-V characteristics of GaAs over Si and concluded that the minimum number of electrical defect centers cause the higher ideality factor, although the quality of the film is very excellent based on the structural and optical results. However, in our case, the GaAs over Ge causes the lattice mismatch only of 0.07% as compared with the system GaAs over Si (4%). This small lattice mismatch or the thermal expansion coefficient mismatch at lower temperatures may create the misfit dislocations, which in turn increases the generation-recombination centers, unless the growth parameters are precisely controlled. Though the film is grown on 2° off-oriented Ge substrate, the measured value of ideality factor is around 1.14, which seems to be very good. The deep level transient spectroscopy (DLTS) curve does not show any peaks and it establishes the absence of such deep levels in the space charge region of the Schottky barrier.

3.4 Richardson Plots:

The Richardson constant A^{**} is usually obtained from the intercept of $\ln(J_s/T^2)$ versus $1000/T$ plots for TE theory and the experimental values should yield a straight line with slope giving the barrier height at 0 K. This plot is shown in Fig. 4 and it is linear only in the temperature range of 160 K to 300 K. The obtained Richardson constant and the zero-bias barrier height values are $0.1356 \text{ AK}^{-2}\text{cm}^{-2}$ and 0.634 eV respectively. As the ideality factor is a strong function of temperature, the modified Richardson plot which is $\ln(J_s/T^2)$ versus $1/nT$ shown in Fig 4 gives $A^{**} = 143.7 \text{ AK}^{-2}\text{cm}^{-2}$ and $\Phi_{b0} = 0.94 \text{ eV}$ (which is in close match with the flat band barrier height of 0.922 eV). It has been reported in literature that the Richardson constant value varies from $3 \text{ AK}^{-2}\text{cm}^{-2}$ to $100 \text{ AK}^{-2}\text{cm}^{-2}$. From the observed A^{**} the corrected A^{**} value can be obtained from the following eqn.

$A^{**}_{\text{corrected}} = A^{**}_{\text{observed}} \exp[q/k(d\phi_b^f/dT)]$ ---(8), where ϕ_b^f is the flat band barrier height. The corrected A^{**} value is $7.039 \text{ AK}^{-2}\text{cm}^{-2}$ which is close to the theoretical value considered for extracting zero-bias barrier height values from Eqn.(2).

4.0 CONCLUSIONS:

The Werner-Gütler model is not adequate to fit the observed data and the homogeneous barrier height & the effective barrier heights are closely matching, which shows the excellent quality of the grown GaAs film. The TE-diffusion conduction mechanism is dominant in the temperature range of 160-300 K and TFE is at lower temperatures. There is no effect of generation-recombination current as there are no deep levels and the defects or the dislocations in the epilayers may not be active. The observed conduction phenomena shows that the GaAs/Ge hetero-structures can withstand the lower temperature range and the quality of the grown GaAs film on Ge substrate is excellent, hence can be used for space solar cells in normal use as well as in low temperature applications.

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